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Design Implementation and Frequency Analysis of Two stage and three stage Operational Amplifiers using C5 process for CMOS

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ABSTRACT: This paper discusses design methodologies and frequency analysis of two stage and three stage i.e. multistage CMOS operational amplifiers and analyse the effect of various parameters on the characteristics of operational amplifiers using submicron CMOS spice models specifically 300 nm C5 process CMOS technology. In this paper response curves are plotted for AC characteristics of 4 different topologies of 2 stage operational amplifiers are tabulated for suitable frequency ranges. Transients are also plotted from nanoseconds scale to microseconds scale. Subsequently FFTs are also tabulated at frequency range from 1 MHz to 25 GHz. By results and reasons it shows that two stage and three stage topologies are suitable choices for low voltage and high performance applications.

Keywords*:* **Operational Amplifiers, CMOS, FFT.**

I. INTRODUCTION

Operational Amplifiers are one of the most widely used building blocks for analog and mixed-signal systems. They are employed from dc bias applications to high speed amplifiers and filters. General purpose op amps can be used as buffers, summers, integrators, differentiators, comparators, negative impedance converters, and many other applications. With the quick improvements of computer aided design (CAD) tools, advancements of semiconductor modelling, steady miniaturization of transistor scaling, and the progress of fabrication processes, the integrated circuit market is growing rapidly. Nowadays, complementary metal-oxide semiconductor (CMOS) technology has become dominant over bipolar technology for analog circuit design in a mixed-signal system due to the industry trend of applying standard process technologies to implement both analog circuits and digital circuits on the same chip. While many digital circuits can be adapted to a smaller device level with a smaller power supply, most existing analog circuitry requires considerable change or even a redesign to accomplish the same feat. With transistor length being scaled down to a few tens of nanometers, analog circuitsare becoming increasingly more difficult to improve upon. The classic Widlar op-amp architecture, originally developed for bipolar devices [10], has required modification for use with CMOS devices. In particular, it has proved difficult to match the open loop gain of bipolar op amps with CMOS technology [3, 4]. This is due to the inherently lower trans-conductance of CMOS devices as well as the gain reduction due to short channel effects that comes into play for submicron CMOS processes.

II. AMPLIFIERS

Operational amplifiers typically are composed of either two or three stages consisting of a differential amplifier, a gain stage and an output stage as seen in Fig. 1. In some applications, the gain stage and the output stage are one and the same if the load is purely capacitive. However, if the output is to drive a resistive load or a large resistive load, then a high current gain buffer amplifier is used at the output. Each stage plays an important role in the performance of the amplifier.

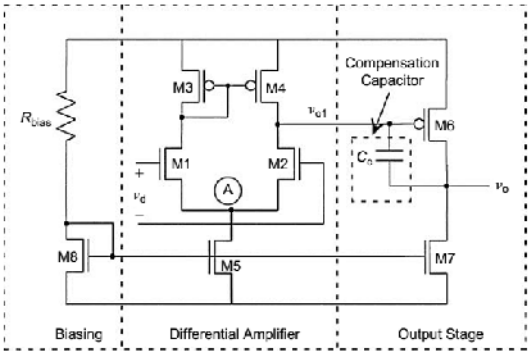

Fig. 1. Basic two stage operational amplifier.

The differential amplifier offers a variety of advantages and is always used as the input to the overall amplifier.

Since it provides common-mode rejection, it eliminates noise common on both inputs, while at the same time amplifying any differences between the inputs. The limit for which this common mode rejection occurs is called common-mode range and signifies the upper and lower common mode signal values for which the devices in the diff-amp are saturated. The differential amplifier also provides gain. The gain stage is typically a common-source or cascade type amplifier. So that the amplifier is stable, a compensation network is used to intentionally lower the gain at higher frequencies. The output stage provides high current driving capability for either driving large capacitive or resistive loads.

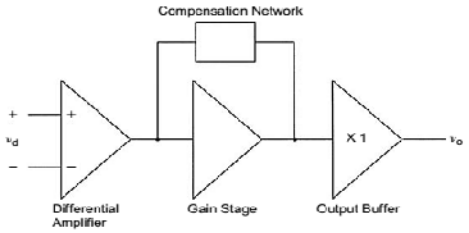

Fig. 2. Block Diagram of a generic amplifier.

The output stage typically will have low output impedance and high signal swing characteristics. In some cases, it may be advantageous to add bipolar devices to improve the performance of the circuitry. These will be presented as the multi stage opamp circuits are analysed.

III. TWO-STAGE CMOS OPERATIONAL AMPLIFIER

Operational Amplifiers are the backbone for many analog circuit designs. Operational amplifiers are one of the basic and important circuits which have a wide application in several analog circuits such as switched capacitor filters, algorithmic, pipelined and sigma delta A/D converter, sample and hold amplifier etc. The speed and accuracy of these circuits depends on the bandwidth and DC gain of the operational amplifiers. Larger the bandwidth and gain, higher the speed and accuracy of the operational amplifier are a critical element in analog sampled data circuit, such as SC filters, modulators [4]. The first block is a differential amplifier. It has two inputs which are the inverting and non-inverting voltage. It provides at the output a differential voltage or a differential current that, essentially, depends on the differential input only. The next block is a differential to single-ended converter. It is used to transform the differential signal generated by the first block into a single ended version. Some architecture doesn't require the differential to single ended function; therefore the block can be excluded. In most cases the gain provided by the input stages is not sufficient and additional amplification is required. This is provided by intermediate stage, which is another differential amplifier, driven by the output of the first stage.

As this stage uses differential input unbalanced output differential amplifier, so it provide required extra gain. The bias circuit is provided to establish the proper operating point for each transistor in its saturation region.

Finally, we have the output buffer stage. It provides the low output impedance and larger output current needed to drive the load of operational amplifier or improves the slew rate of the operational amplifier. Even the output stage can be dropped: many integrated applications do not need low output impedance; moreover, the slew rate permitted by the gain stage can be sufficient for the application. If the operational amplifier is intended to drive a small purely capacitive load, which is the case in many switched capacitor or data conversion applications, the output buffer is not used. When the output stage is not used the circuit, it is an operational transconductance amplifier, OTA. The purpose of the compensation circuit is lower the gain at high frequencies and to maintain stability when negative feedback is applied to the operational amplifier [7].

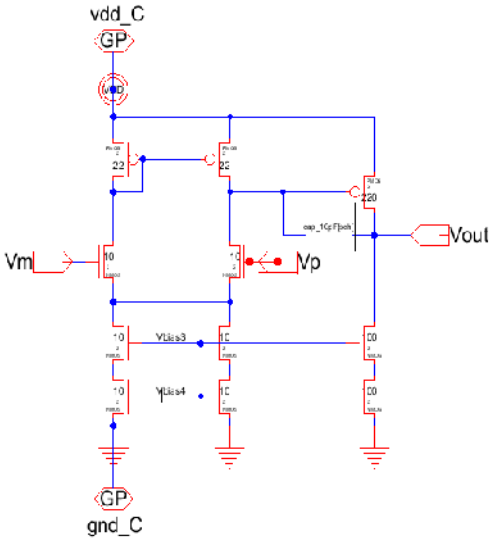

Fig. 3. Schematic for topology 1 for two stage operational amplifier.

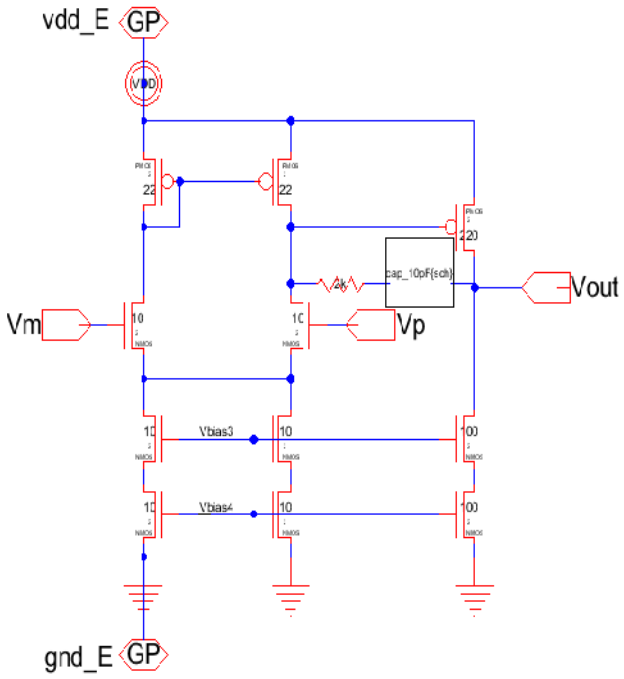

Fig. 4. Schematic for topology 2, 2 stage operational amplifier.

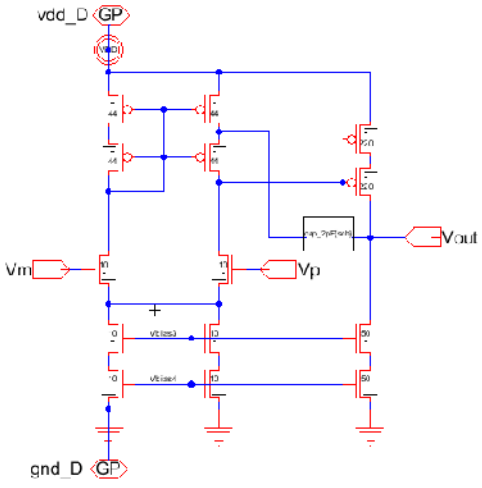

Fig. 5. Schematic for topology 3, two stage operational amplifier.

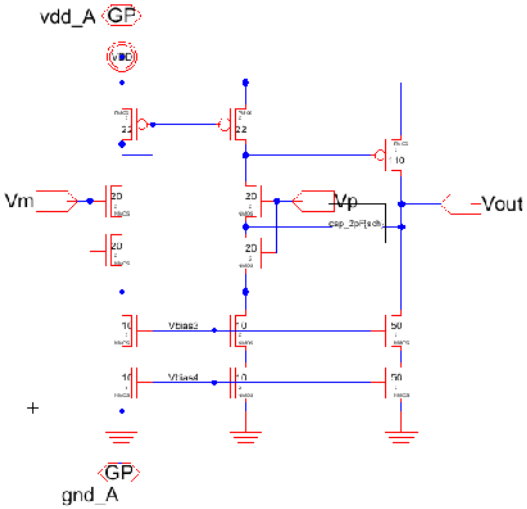

Fig.6. Schematic for topology 4, two stage operational amplifier.

IV. THREE-STAGE CMOS OPERATIONAL AMPLEFIER

Three stage operational amplifiers are used in applications where low power is required or that can operate with low supply voltage or with minimal power from VDD. In comparison to two –stage operational amplifiers the bias circuit is to be developed can pull more current from VDD than the operational amplifiers it biases. So I have used two circuit architectures for biasing circuits.

For proper operation of the output stage floating current sources are generally preferred. Towards keeping a large gain and lowering the power supply voltage, considering the three stage operational amplifier above. The design is cascade of two different differential amplifier stages followed by a common source amplifier. If we connect a resistive load to the output of the common source stage, the overall operational amplifier gain remains relatively high due to the cascaded gain of two differential amplifier stages. This topology of operational amplifier i.e. more than two stages is a sort of compensation. The compensation of capacitors within the operational amplifier for overall improvement in the desired operational amplifier characteristics[3,6].

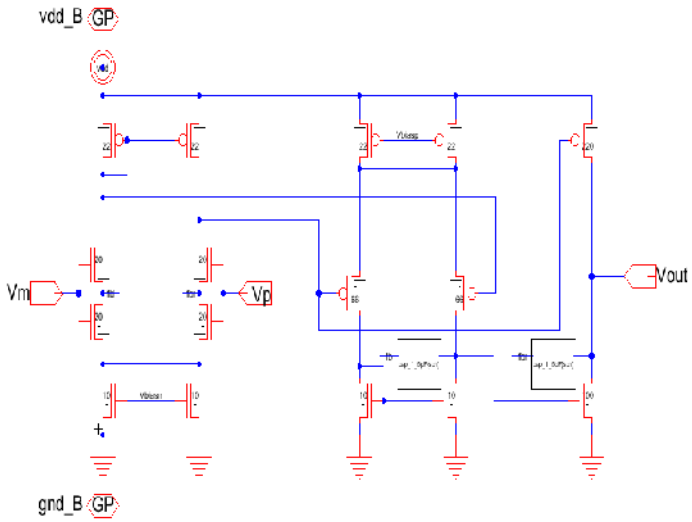

Fig. 7. Schematic for topology 3, two stage operational amplifier.

V. DESIGN METHODOLOGY AND DESIGN FLOW

It is assumed that all transistors are in saturation for the above relationships. The design in this project is a two-stage op amp with an n-channel input pair. The op amp uses a dual-polarity power supply (Vdd and Vss) so the ac signals can swing above and below ground and also be centered at ground.[38] Design flow approach regarding the same is as follows

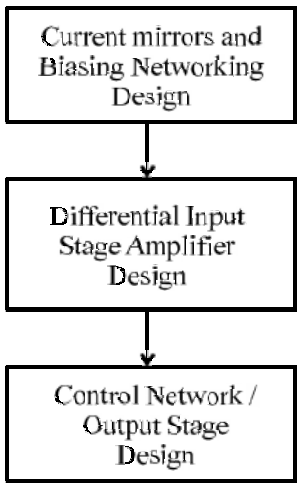

Fig. 8. Design Flow used for OpAmp Design.

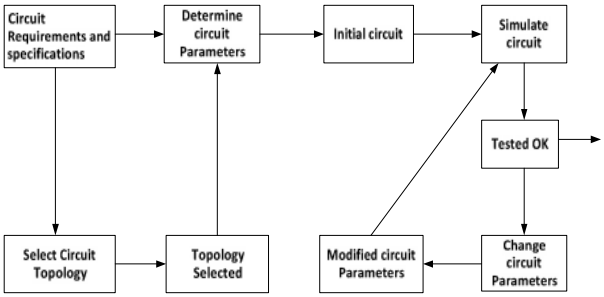

Fig. 9. Design Procedure.

VI. SIMULATION RESULTS AND FFT PLOTS

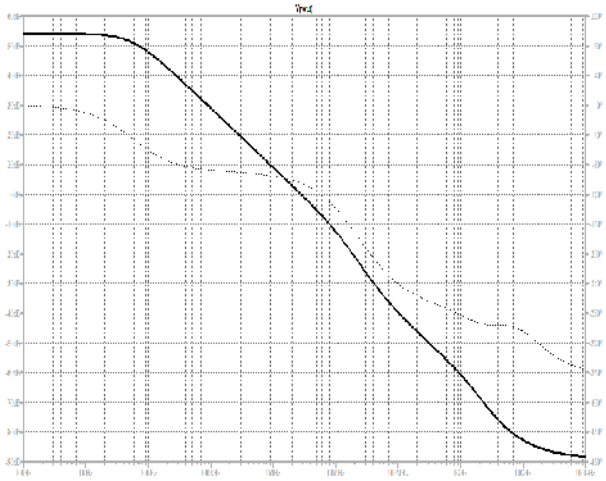

Fig. 10. AC Simulation plot for topology 1 , 2 stage CMOS operational amplifier.

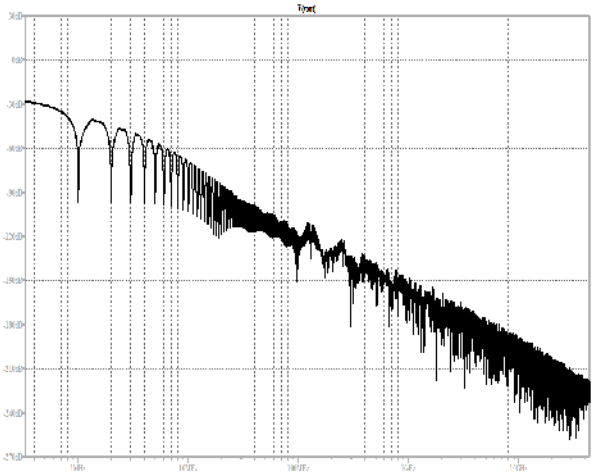

Fig. 11. FFT Analysis plot for topology 1, 2 stage CMOS Operational Amplifier.

Table 1: Table enlisting Frequency, Magnitude, Phase and Group Delay topology 1, 2 stage CMOS Operational Amplifier.

S.No.	Frequency	Magnitude	Phase	Group Delay
1.	1MHz	--86.207dB	345.40°	55.021 ns
2.	10 MHz	-84..88 dB	164.55°	-146.52 ns
3.	100 MHz	-124.82 dB	-2.071°	-76.89 ns
4.	1 GHz	-161.29 dB	-1.65°	924.655ns
5.	10GHz	-207.39 dB	-1.95°	856.84 ns
6.	25 GHz	-217.83 dB	-359.04°	-99.69 ns

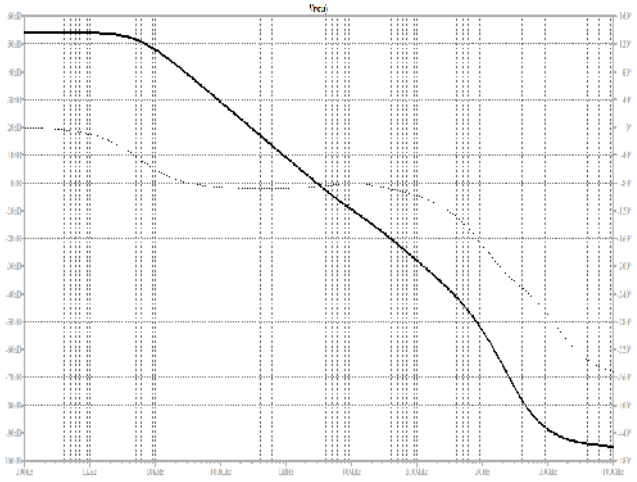

Fig. 12. AC Simulation plot for topology 2, 2 stage CMOS operational amplifier.

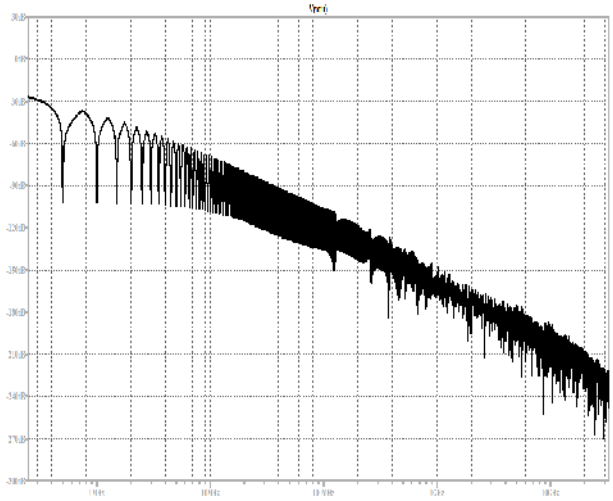

Fig. 13. FFT Analysis plot for topology 2, 2 stage CMOS Operational Amplifier.

Table 2: Table enlisting Frequency, Magnitude, Phase and Group Delay for topology 2, 2 stage CMOS Operational Amplifier.

S.No.	Frequency	Magnitude	Phase	Group Delay
1.	1MHz	-87.20 dB	-11.62°	49.03 ns
2.	10 MHz	-84.13 dB	-45.73°	-62.54ns
3.	100 MHz	-109.13 dB	-108.5 °	339.52 ns
4.	1 GHz	-154.56 dB	51.54°	309.59 ns
5.	10GHz	-198.91 dB	-59.78°	665.65 ns
6.	25 GHz	-222.12 dB	7.041°	116.341ns

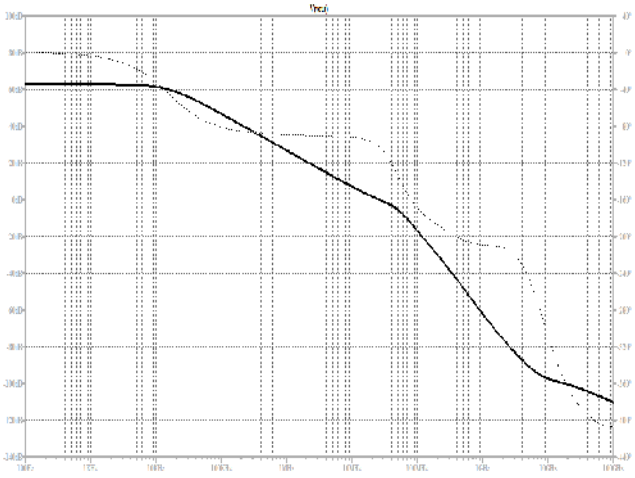

Fig.14. AC Simulation plot for topology 3, 2 stage CMOS operational amplifier.

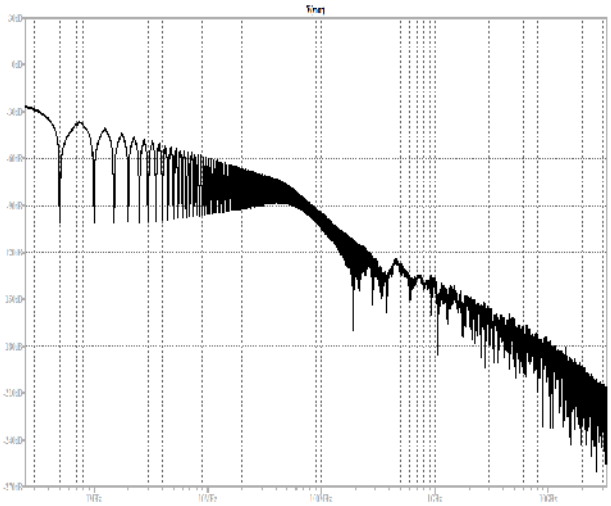

Fig. 15. FFT Analysis plot for topology 3, 2 stage CMOS Operational Amplifier.

Table 3: Table enlisting Frequency, Magnitude, Phase and Group Delay for topology 3, 2 stage CMOS Operational Amplifier.

S.No.	Frequency	Magnitude	Phase	Group Delay
1.	1MHz	-86.23 dB	5.50°	8.16 ns
2.	10 MHz	-73.97 dB	39.26 °	161.287 ns
3.	100 MHz	-96.67 dB	-98.01°	-323.33 ns
4.	1 GHz	-139.74 dB	-131.42 °	-392.67 ns
5.	10GHz	-187.82 dB	35.98°	-382.96 ns
6.	25 GHz	-214.49 dB	-124.53°	55.08 ns

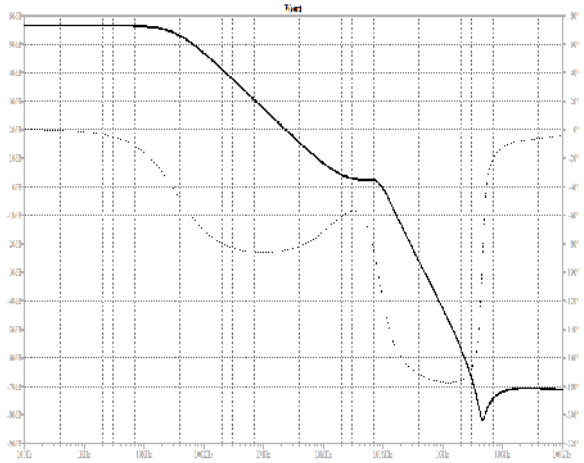

Fig. 16. AC Simulation plot for for topology 4, 2 stage CMOS operational amplifier.

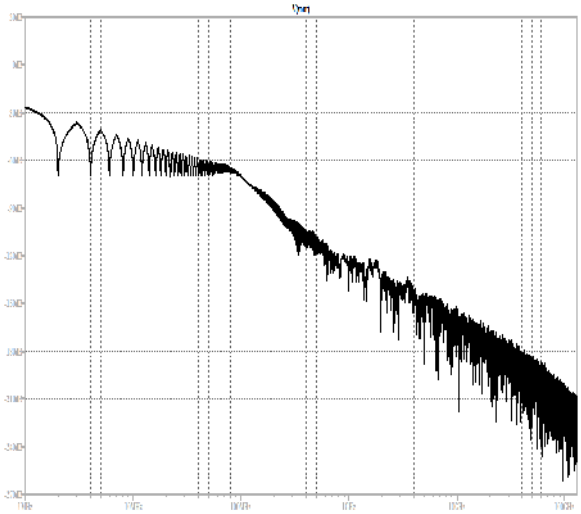

Fig.17. FFT Analysis plot for topology 4, 2 stage CMOS Operational Amplifier.

Table 4: Table enlisting Frequency, Magnitude, Phase and Group Delay for topology 4, 2 stage CMOS Operational Amplifier.

S.No.	Frequency	Magnitude	Phase	Group Delay
1.	1MHz	-26.94 dB	-162.92°	-45.80 ns
2.	10 MHz	-66.65 dB	-19.82 °	-48.92 ns
3.	100 MHz	-70.35 dB	11.41 °	-151.26 ns
4.	1 GHz	-132.04 dB	120.088°	-21.604 ns
5.	10GHz	-164.36 dB	9.63°	-38.66 ns
6.	25 GHz	-183.82 dB	-48.58°	-57.73 ns

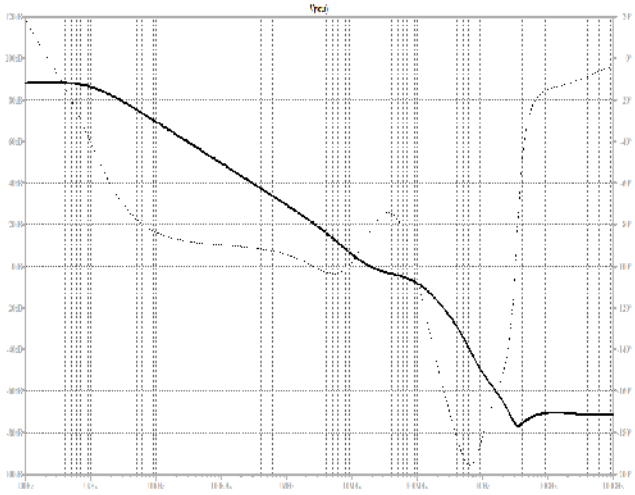

Fig. 18. AC Simulation plot for 3 stage CMOS operational amplifier.

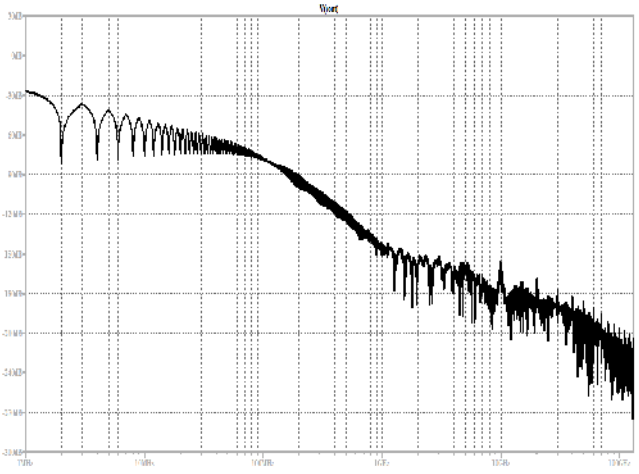

Fig. 19. FFT Analysis plot for 3 stage CMOS Operational Amplifier.

Table 5: Table enlisting Frequency, Magnitude, Phase and Group Delay, 3 stage CMOS Operational Amplifier.

S.No.	Frequency	Magnitude	Phase	Group Delay
1.	1MHz	-26.942 dB	-164.36°	-157.98 ns
2.	10 MHz	-71.027 dB	15.88°	-39.72 ns
3.	100 MHz	-77.85 dB	9.38 °	-130.78 ns
4.	1 GHz	-143.60 dB	16.36°	188.15ns
5.	10GHz	-159.9 dB	-110.32°	-46.64 ns
6.	25 GHz	-189.91 dB	9.81°	30.04 ns

VII. CONCLUSION

Keeping in view different applications the Op-amp has been designed. For this first a selection is made for the active device used. Four different topologies of 2 stage operational amplifiers are analyzed for various transients and FFT responses are calculated for frequencies ranging from 1 MHz to 25 MHz. AC analysis and Quiscent point analysis is also done for all the mentioned topologies. The development of a design procedure provides a quick, well integrated and effective mechanism for estimation and calculation of various parameters. The steps highlighted make it easy to redesign the circuit for various set of specifications. The responses are simulated using LTSpice and Electric VLSI CAD design tool. The simulated results of the Op-amp are in compliance with the theoretical values.

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